IN THE CLAIMS:

Please cancel Claim 40 without prejudice or disclaimer of the subject matter recited therein.

Please amend Claims 1-15, 20, 21, 26, 31-33 and 41-44 as follows.

1. (Currently Amended) A ~~demodulator~~ system for demodulating digital data, comprising:

a receiver circuit for receiving a transmitted digital data signal;

a correlator to correlate the transmitted digital data signal received from said receiver circuit with a predefined reference training sequence to produce [[a]] correlation ~~value~~ values;

a verification unit to select correlation values above a threshold value;

a determining device to determine if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing and to calculate a required fractional sample delay to improve synchronization;

an implementing device implementing the calculated fractional sample delay if said determining device determines that the fractional sample delay would improve the demodulation synchronization timing; and

a demodulating device for demodulating the transmitted digital data signal outputted from said implementing device.

2. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 1, wherein said determining device comprises an algorithm that determines if the fractional sample delay would improve the demodulation synchronization timing.

3. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 2, wherein the algorithm comprises exploiting the geometry of a correlation curve to determine if the fractional sample delay would improve the demodulation synchronization timing.

4. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 3, wherein the algorithm further comprises comparing first and last correlation values of the correlation curve that exceed the threshold value.

6 5. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 3, wherein the algorithm further comprises counting correlation values of the correlation curve that exceed the threshold value.

5 6. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 4, wherein said determining device determines the required fractional sample delay based on the selected correlation values.

7. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 5, wherein said determining device determines the required fractional sample delay based on the selected correlation values.

8. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 1, wherein the fractional sample delay is in the range of -0.5 to 0.5.

9. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 8, wherein the fractional sample delay is selected from the group consisting of ± ¼ and ½.

10. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 1, wherein said implementing device comprises an interpolation filter that implements the fractional sample delay.

11. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 10, wherein the interpolation filter includes (i) a multiplier for multiplying first and second samples of each pair of input samples by respective coefficients to obtain two fractional values, and (ii) an ~~adder/summer~~ adder or summer for summing the fractional values.

12. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 11, wherein said implementing device uses respective coefficients of 0.5 and 0.5 to implement a fractional sample delay of ½ sample.

13. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 11, wherein said implementing device uses respective coefficients of 1.0 and 0.0 to implement a fractional sample delay of 0 ~~samples~~ sample.

14. (Currently Amended) A ~~demodulator~~ system for demodulating digital data according to Claim 1, wherein said demodulator comprises a demodulator portion of a VHF Digital Link Mode 2 receiver.

17 ~~15~~. (Currently Amended) A method for demodulating digital data, comprising the steps of:

receiving a digital data signal;

correlating the received digital data signal with a predefined reference training sequence to produce a correlation value;

selecting correlation values above a threshold value;

determining if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing and calculating a required fractional sample delay to improve synchronization;

implementing the fractional sample delay if it is determined in said determining step that the fractional sample delay would improve the demodulation synchronization timing; and

demodulating the implemented received digital data signal.

18 16. (Previously Presented) A method for demodulating digital data according to Claim 15, 17 wherein said determining step comprises an algorithm that determines if the fractional sample delay would improve the demodulation synchronization timing.

19 17. (Previously Presented) A method for demodulating digital data according to Claim 16, 18 wherein the algorithm comprises exploiting the geometry of a correlation curve to determine in said determining step if the fractional sample delay would improve the demodulation synchronization timing.

20 18. (Previously Presented) A method for demodulating digital data according to Claim 17, 19 wherein the algorithm further comprises comparing first and last correlation values of the correlation curve that exceed the threshold value.

22 19. (Previously Presented) A method for demodulating digital data according to Claim 17, 19 wherein the algorithm further comprises counting correlation values of the correlation curve that exceed the threshold value.

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20. (Currently Amended) A method for demodulating digital data according to Claim 18, wherein said determining step further determines the required fractional sample delay based on the selected correlation values.

23
21. (Currently Amended) A method for demodulating digital data according to Claim 19, wherein said determining step further determines the required fractional sample delay based on the selected correlation values.

24
22. (Original) A method for demodulating digital data according to Claim 17
15, wherein the fractional sample delay is in the range of -0.5 to 0.5.

25
23. (Original) A method for demodulating digital data according to Claim 24
22, wherein the fractional sample delay is selected from the group consisting of ± ¼ and ½.

26
24. (Previously Presented) A method for demodulating digital data according to Claim 17
15, wherein said implementing step includes an interpolation step using an interpolation filter to implement the fractional sample delay.

27
25. (Previously Presented) A method for demodulating digital data according to Claim 26
24, wherein the interpolation step comprises the steps of (i) providing input

samples and multiplying first and second samples of each pair of the input samples by respective coefficients to obtain two fractional values, and (ii) summing the fractional values.

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26. (Currently Amended) A method for demodulating digital data according to Claim 25, 27 wherein the fractional sample delay of 0 ~~samples~~ sample is implemented in said implementing step by using respective coefficients of 1.0 and 0.0.

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27. (Previously Presented) A method for demodulating digital data according to Claim 25, 27 wherein the fractional sample delay of ½ sample is implemented in said implementing step by using respective coefficients of 0.5 and 0.5.

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28. (Previously Presented) A method for demodulating digital data according to Claim 15, 17 wherein a VHF Digital Link Mode 2 radio receiver is provided for implementing the method.

31
29. (Original) A method for demodulating digital data according to Claim 15, 17 wherein a digital circuit is provided for implementing the method.

32
30. (Original) A method for demodulating digital data according to Claim 15, 17 wherein a process is provided for implementing the method.

33
31. (Currently Amended) Computer executable code stored in a computer readable medium for implementing a method for demodulating digital data, said code for executing the steps comprising:

receiving a digital data signal;

correlating the received digital data signal with a predefined reference training sequence to produce a correlation value;

selecting correlation values above a threshold value;

determining if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing and calculating a required fractional sample delay to improve synchronization;

implementing the fractional sample delay if it is determined in said determining step that [[a]] the fractional sample delay would improve the demodulation synchronization timing; and

demodulating the implemented received digital data signal.

34
32. (Currently Amended) Computer executable code for implementing a method for demodulating digital data according to Claim 33 31, wherein said determining step comprises an algorithm that determines if [[a]] the fractional sample delay would improve the demodulation synchronization timing.

35. (Currently Amended) Computer executable code for implementing a method for demodulating digital data according to Claim 34, wherein the algorithm comprises exploiting the geometry of a correlation curve to determine in said determining step if [[a]] the fractional sample delay would improve the demodulation synchronization timing.

36. (Original) Computer executable code for implementing a method for demodulating digital data according to Claim 35, wherein the algorithm further comprises comparing first and last correlation values of the correlation curve that exceed a threshold value.

38. (Original) Computer executable code for implementing a method for demodulating digital data according to Claim 35, wherein the algorithm further comprises counting correlation values of the correlation curve that exceed a threshold value.

37. (Previously Presented) Computer executable code for implementing a method for demodulating digital data according to Claim 36, wherein said determining step further determines the required fractional sample delay based on the selected correlation values.

39. (Previously Presented) Computer executable code for implementing a method for demodulating digital data according to Claim 38, wherein said determining step further determines the required fractional sample delay based on the selected correlation values.

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38. (Previously Presented) Computer executable code for implementing a method for demodulating digital data according to Claim 33, wherein said implementing step includes an interpolation step using an interpolation filter to implement the fractional sample delay.

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39. (Previously Presented) Computer executable code for implementing a method for demodulating digital data according to Claim 40, wherein the interpolation step comprises the steps of (i) multiplying first and second samples of each pair of input samples by respective coefficients to obtain two fractional values, and (ii) summing the fractional values.

Claim 40. (Cancelled).

42
41. (Currently Amended) A method for demodulating digital data, comprising the steps of:

receiving a digital data signal;

correlating the received digital data signal with a predefined reference training sequence to produce a correlation value;

selecting correlation values above a threshold value;

determining an amount of fractional sample delay to be added to a demodulator's symbol sampling timing based on the selected correlation values;

implementing the amount of fractional sample delay; and

demodulating the implemented received digital data signal.

43
42. (Currently Amended) A demodulator for demodulating digital data, comprising:

receiving means for receiving a digital data signal;

correlating means for correlating the digital data signal received from said receiving means with a predefined reference training sequence to produce a correlation value;

verification means to select correlation values above a threshold value;

determining means for determining an amount of a fractional sample delay to be added to a demodulator's symbol sampling timing based on the selected correlation values;

implementing means for implementing the amount of fractional sample delay; and

demodulating means for demodulating the digital data signal outputted from said implementing means.

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43. (Currently Amended) A modulator for demodulating digital data according to Claim 1, wherein said correlator receives the predefined reference training sequence at the beginning of each transmission.

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~~44~~. (Currently Amended) A modulator for demodulating digital data according to Claim ~~43~~, wherein the predefined reference training sequence identifies the
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transmitted digital data signal as a VDL Mode 2 signal.